ABSTRACT OF THE DISCLOSURE

A core-based multi-bit memory (400) having a dual-bit dynamic referencing architecture (408, 410) fabricated on the memory core (401). A first reference array (408) and a second reference array (410) are fabricated on the memory core (401) such that a reference cell pair (185) comprising one cell (182) of the first reference array (408) and a corresponding cell (184) of the second reference array (410) are read and averaged to provide a reference voltage for reading a data array(s).